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Lisa K. Jorgenson, Esq.
STMicroelectronics, Inc.
1310 Electronics Drive
Carrollton, TX 75006

EXAMINER	
CLEARY, THOMAS J	

ART UNIT	PAPER NUMBER
2111	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/060,454	MUROOR, SRIKANTH R.	
	Examiner	Art Unit	
	Thomas J. Cleary	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 January 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the Applicant regards as his invention.

2. Claims 1-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

3. The term "slowly" in Claims 1, 9, and 17 is a relative term which renders the claim indefinite. The term "slowly" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

4. The term "rapidly" in Claims 1, 9, and 17 is a relative term which renders the claim indefinite. The term "rapidly" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 9 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent Number 6,163,850 to Wood ("Wood").

7. In reference to Claim 9, Wood teaches a shared bus system (See Column 1 Lines 9-14) comprising: N bus devices capable of requesting access to a shared bus (See Figure 1 and Column 2 Lines 6-15); M tristate line drivers (See Figures 1, 2, and 3B Number 20), each of said M tristate line drivers having an input for receiving a logic bit from one of said N bus devices and an output for outputting said received logic bit to said shared bus (See Figure 3B), wherein said each tristate line driver outputs said received logic bit when a line driver enable signal associated with said each tristate line driver is enabled and an output of said each tristate line driver is put into a high-impedance state when said line driver enable signal is disabled (See Column 2 Lines 6-15); a bus arbitrator operable to slowly activate and rapidly de-activate said M tristate line drivers (See Figure 3B and Column 2 Lines 6-15), said bus arbitrator comprising: an input interface capable of receiving an Enable_clock_drive signal, which is equivalent to

a first bus access request signal, from a first of said N bus devices (See Figure 3B); a delay circuit capable of receiving said first bus access request signal from said input interface and generating therefrom a time-delayed first bus access request signal (See Figure 3B Numbers 62 and Column 3 Lines 43-52); and a comparator circuit capable of receiving said first bus access request signal from said input interface and said time-delayed first bus access request signal from said delay circuit and generating a line driver enable signal only if both of said first bus access request signal and said time-delayed first bus access request signal are enabled (See Figure 3B Number 60 and Column 3 Lines 43-52); and a bus keeper capable of holding each line of the shared bus at a particular logic level when all of the tristate line drivers are put into the high-impedance state (See Figure 3B Number 66 and Column 3 Lines 41-42).

8. In reference to Claim 10, Wood teaches the limitations as applied to Claim 9 above. Because Wood teaches using an AND gate as the comparator circuit for comparing the first bus access request signal and the delayed first bus access request signal, the line driver enable signal, which is the output of the AND gate, will inherently be disabled if either of the first bus access request signal or the delayed first bus access request signal is disabled, since the output of an AND gate is only enabled when both of its inputs are enabled (See Figure 3B Number 60 and Column 3 Lines 43-52).

9. In reference to Claim 11, Wood teaches the limitations as applied to Claim 10 above. The time delay of the delay circuit is equal to the time required for the signal to

propagate through the flip-flops comprising the delay circuit, which is inherently much greater than the maximum de-activation delay period, which is equivalent to the switching time of the AND gate.

10. In reference to Claim 12, Wood teaches the limitations as applied to Claim 11 above. Wood further teaches that said comparator circuit comprises an AND gate having a first input for receiving said first bus access request and a second input for receiving said time-delayed first bus access request signal (See Figure 3B Number 60 and Column 3 Lines 43-52).

11. In reference to Claims 15 and 16, Wood teaches the limitations as applied to Claim 11 above. Wood further teaches that said delay circuit is a synchronous delay circuit comprising a flip-flop having an input capable of receiving said first bus access request signal from said input interface and an output coupled to said comparator circuit that generates said time-delayed first bus access request signal (See Figure 3B Number 62; Column 3 Lines 43-52; and Column 4 Lines 18-20).

12. In reference to Claim 17, Wood teaches a method for slowly activating and rapidly de-activating a plurality of tristate line drivers coupled between the shared bus and the N bus devices (See Figures 1, 2, and 3B Number 20; Column 1 Lines 9-14; and Column 2 Lines 6-15), the method comprising the steps of: receiving an Enable_clock_drive signal, which is equivalent to a first bus access request signal, from

a first of the plurality of bus devices (See Figure 3B); generating from the first bus access request signal a time-delayed first bus access request signal (See Figure 3B Numbers 62 and Column 3 Lines 43-52); comparing in a comparator circuit the first bus access request signal and the time-delayed first bus access request signal and generating a line driver enable signal only if both of the first bus access request signal and the time-delayed first bus access request signal are enabled (See Figure 3B Number 60 and Column 3 Lines 43-52); and holding each line of the shared bus at a particular logic level when all of the tristate line drivers are put into a high-impedance state (See Figure 3B Number 66 and Column 3 Lines 41-42).

13. In reference to Claim 18, Wood teaches the limitations as applied to Claim 17 above. Because Wood teaches using an AND gate as the comparator circuit for comparing the first bus access request signal and the delayed first bus access request signal, the line driver enable signal, which is the output of the AND gate, will inherently be disabled if either of the first bus access request signal or the delayed first bus access request signal is disabled, since the output of an AND gate is only enabled when both of its inputs are enabled (See Figure 3B Number 60 and Column 3 Lines 43-52).

14. In reference to Claim 19, Wood teaches the limitations as applied to Claim 18 above. The time delay of the delay circuit is equal to the time required for the signal to propagate through the flip-flops comprising the delay circuit, which is inherently much

greater than the maximum de-activation delay period, which is equivalent to the switching time of the AND gate.

15. In reference to Claim 20, Wood teaches the limitations as applied to Claim 19 above. Wood further teaches that said comparator circuit comprises an AND gate having a first input for receiving said first bus access request and a second input for receiving said time-delayed first bus access request signal (See Figure 3B Number 60 and Column 3 Lines 43-52).

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 1-4, 7-8, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art ("AAPA") and Wood.

18. In reference to Claim 1, AAPA teaches a shared bus system comprising a plurality of bus devices capable of requesting access to a shared bus (See Figure 2), a bus arbitrator (See Figure 2 Number 210) operable to slowly activate and rapidly de-

activate tristate line drivers (See Figure 2 Numbers 230A and 230B) coupled to said shared bus (See Figure 2 Number 240), said bus arbitrator comprising: an input circuit (See Figure 2 Numbers 215 and 220) capable of receiving a first bus access request signal (See Figure 2 'REQ1') from a first of said plurality of bus devices and a second bus access request signal (See Figure 2 'REQ2') from a second of said plurality of bus devices, the input circuit also capable of outputting the second bus access request signal when the first bus access request signal is not enabled and blocking the second bus access request signal when the first bus access request signal is enabled (See Figure 2 Numbers 215 and 220). AAPA does not teach a delay circuit capable of receiving a first bus access request signal and generating therefrom a time-delayed first bus access request signal; and a comparator circuit capable of receiving said first bus access request signal and said time-delayed first bus access request signal and generating a line driver enable signal only if both of said first bus access request signal and said time-delayed first bus access request signal are enabled. Wood teaches a delay circuit capable of receiving a bus access request signal and generating therefrom a time-delayed bus access request signal (See Figure 3B Number 62 and Column 3 Lines 43-52); and a comparator circuit capable of receiving said bus access request signal and said time-delayed bus access request signal and generating a line driver enable signal only if both of said bus access request signal and said time-delayed bus access request signal are enabled (See Figure 3B Number 60 and Column 3 Lines 43-52).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of AAPA with the delay system of Wood, resulting in the invention of Claim 1, in order to supply a delay between termination of control of the bus by one device and enabling of control of the bus by another device, the preventing contention and reducing power loss due to multiple enabled devices (See Column 3 Lines 43-52).

19. In reference to Claim 2, AAPA and Wood teach the limitations as applied to Claim 1 above. Wood further teaches using an AND gate as the comparator circuit for comparing the bus access request signal and the delayed bus access request signal, and thus the line driver enable signal, which is the output of the AND gate, will inherently be disabled if either of the bus access request signal or the delayed bus access request signal is disabled, since the output of an AND gate is only enabled when both of its inputs are enabled (See Figure 3B Number 60 and Column 3 Lines 43-52).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of AAPA with the delay system of Wood, resulting in the invention of Claim 2, in order to supply a delay between termination of control of the bus by one device and enabling of control of the bus by another device, the preventing contention and reducing power loss due to multiple enabled devices (See Column 3 Lines 43-52).

20. In reference to Claim 3, AAPA and Wood teach the limitations as applied to Claim 2 above. Wood further teaches that the time delay of the delay circuit is equal to the time required for the signal to propagate through the flip-flops comprising the delay circuit, which is inherently much greater than the maximum de-activation delay period, which is equivalent to the switching time of the AND gate (See Figure 3B and Column 3 Lines 43-52).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of AAPA with the delay system of Wood, resulting in the invention of Claim 3, in order to supply a delay between termination of control of the bus by one device and enabling of control of the bus by another device, the preventing contention and reducing power loss due to multiple enabled devices (See Column 3 Lines 43-52).

21. In reference to Claim 4, AAPA and Wood teach the limitations as applied to Claim 3 above. Wood further teaches that said comparator circuit comprises an AND gate having a first input for receiving said bus access request and a second input for receiving said time-delayed bus access request signal (See Figure 3B Number 60 and Column 3 Lines 43-52).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of AAPA with the delay system of Wood, resulting in the invention of Claim 4, in order to supply a delay between termination of control of the bus by one device and enabling of control of the bus by another device,

the preventing contention and reducing power loss due to multiple enabled devices (See Column 3 Lines 43-52).

22. In reference to Claims 7 and 8, AAPA and Wood teach the limitations as applied to Claim 3 above. Wood further teaches that said delay circuit is a synchronous delay circuit comprising a flip-flop having an input capable of receiving said bus access request signal and an output coupled to said comparator circuit that generates said time-delayed bus access request signal (See Figure 3B Number 62; Column 3 Lines 43-52; and Column 4 Lines 18-20).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of AAPA with the delay system of Wood, resulting in the invention of Claim 7-8, in order to supply a delay between termination of control of the bus by one device and enabling of control of the bus by another device, the preventing contention and reducing power loss due to multiple enabled devices (See Column 3 Lines 43-52).

23. In reference to Claim 21, AAPA and Wood teach the limitations as applied to Claim 1 above. AAPA further teaches that the input circuit comprises an inverter capable of receiving and inverting the first bus access request signal (See Figure 2 Number 215); and an AND gate capable of receiving the inverted first bus access request signal and the second bus access request signal (See Figure 2 Number 220), the AND gate also capable of outputting the second bus access request signal when the

first bus access request signal is not enabled and blocking the second bus access request signal when the first bus access request signal is enabled (See Figure 2 Number 210).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of AAPA with the delay system of Wood, resulting in the invention of Claim 21, in order to supply a delay between termination of control of the bus by one device and enabling of control of the bus by another device, the preventing contention and reducing power loss due to multiple enabled devices (See Column 3 Lines 43-52).

24. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA and Wood as applied to Claim 3 above, and further in view of US Patent Number 5,306,963 to Leak et al. ("Leak").

25. In reference to Claims 5 and 6, AAPA and Wood teach the limitations as applied to Claim 3 above. AAPA and Wood do not teach that the delay circuit is an asynchronous delay circuit comprising an even number of inverters connected in series, wherein a first of said even number of inverters receives said first bus access request signal and a last of said even number of inverters generates said time-delayed first bus access request signal. Leak teaches an asynchronous delay chain comprising an even number of inverters wherein the first inverter in the chain receives a signal at its input

and the last inverter in the chain generates a time-delayed version of the input signal (See Figure 1 and Column 4 Lines 3-37).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of AAPA and Wood using the delay chain of Leak, resulting in the inventions of Claims 5 and 6, because a delay chain is simpler to construct than a flip-flop; a delay chain does not require a clock signal; and the switching time of an inverter in a delay chain is faster than the clock signal used by a flip-flop, thus providing a higher resolution when setting the delay time. Further, the delay chain of Leak is used for an equivalent purpose as the delay circuit of Wood, namely providing a signal to one input of a comparison circuit and providing a delayed version of said signal to the other input of said comparison circuit (See Figure 1 and Column 4 Lines 3-55 of Leak; and Figure 3B and Column 3 Lines 43-52 of Wood).

26. Claims 1-4, 7-8, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA and US Patent Number 5,044,167 to Champagne ("Champagne").

27. In reference to Claim 1, AAPA teaches a shared bus system comprising a plurality of bus devices capable of requesting access to a shared bus (See Figure 2), a bus arbitrator (See Figure 2 Number 210) operable to slowly activate and rapidly de-activate tristate line drivers (See Figure 2 Numbers 230A and 230B) coupled to said shared bus (See Figure 2 Number 240), said bus arbitrator comprising: an input circuit

(See Figure 2 Numbers 215 and 220) capable of receiving a first bus access request signal (See Figure 2 'REQ1') from a first of said plurality of bus devices and a second bus access request signal (See Figure 2 'REQ2') from a second of said plurality of bus devices, the input circuit also capable of outputting the second bus access request signal when the first bus access request signal is not enabled and blocking the second bus access request signal when the first bus access request signal is enabled (See Figure 2 Numbers 215 and 220). AAPA does not teach a delay circuit capable of receiving a first bus access request signal and generating therefrom a time-delayed first bus access request signal; and a comparator circuit capable of receiving said first bus access request signal and said time-delayed first bus access request signal and generating a line driver enable signal only if both of said first bus access request signal and said time-delayed first bus access request signal are enabled. Champaign teaches a delay circuit capable of receiving a signal and generating therefrom a time-delayed signal (See Figure 2 Number 114 and Column 5 Lines 40-48); and a comparator circuit capable of receiving said signal and said time-delayed signal and generating a line driver enable signal only if both of said signal and said time-delayed signal are enabled (See Figure 2 Number 112 and Column 5 Lines 40-48).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of AAPA with the delay system of Champaign, resulting in the invention of Claim 1, in order to provide a debounce delay period and thus increase the fault tolerance of the signal (See Column 5 Lines 44-49 of Champaign).

28. In reference to Claim 2, AAPA and Champaign teach the limitations as applied to Claim 1 above. Champaign further teaches using an AND gate as the comparator circuit for comparing the signal and the delayed signal, and thus the output of the AND gate will inherently be disabled if either the signal or the delayed signal is disabled, since the output of an AND gate is only enabled when both of its inputs are enabled (See Figure 2 Number 112 and Column 5 Lines 43-48).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of AAPA with the delay system of Champaign, resulting in the invention of Claim 2, in order to provide a debounce delay period and thus increase the fault tolerance of the signal (See Column 5 Lines 44-49 of Champaign).

29. In reference to Claim 3, AAPA and Champaign teach the limitations as applied to Claim 2 above. Champaign further teaches that the time delay of the delay circuit is equal to 1 second, which is inherently much greater than the maximum de-activation delay period, which is equivalent to the switching time of the AND gate (See Figure 2 Number 114 and Column 5 Lines 44-48).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of AAPA with the delay system of Champaign, resulting in the invention of Claim 3, in order to provide a debounce delay

period and thus increase the fault tolerance of the signal (See Column 5 Lines 44-49 of Champaign).

30. In reference to Claim 4, AAPA and Champaign teach the limitations as applied to Claim 3 above. Champaign further teaches that said comparator circuit comprises an AND gate having a first input for receiving said signal and a second input for receiving said time-delayed signal (See Figure 2 Number 112 and Column 5 Lines 43-52).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of AAPA with the delay system of Champaign, resulting in the invention of Claim 4, in order to provide a debounce delay period and thus increase the fault tolerance of the signal (See Column 5 Lines 44-49 of Champaign).

31. In reference to Claims 7 and 8, AAPA and Champaign teach the limitations as applied to Claim 3 above. Champaign further teaches that said delay circuit is a synchronous delay circuit which inherently comprises a flip-flop having an input capable of receiving said first signal and an output coupled to said comparator circuit that generates said time-delayed first signal (See Figure 2 Number 114 and Column 5 Lines 45-51).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of AAPA with the delay system of Champaign, resulting in the inventions of Claims 7 and 8, in order to provide a

debounce delay period and thus increase the fault tolerance of the signal (See Column 5 Lines 44-49 of Champaign).

32. In reference to Claim 21, AAPA and Champaign teach the limitations as applied to Claim 1 above. AAPA further teaches that the input circuit comprises an inverter capable of receiving and inverting the first bus access request signal (See Figure 2 Number 215); and an AND gate capable of receiving the inverted first bus access request signal and the second bus access request signal (See Figure 2 Number 220), the AND gate also capable of outputting the second bus access request signal when the first bus access request signal is not enabled and blocking the second bus access request signal when the first bus access request signal is enabled (See Figure 2 Number 210).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of AAPA with the delay system of Champaign, resulting in the invention of Claim 21, in order to provide a debounce delay period and thus increase the fault tolerance of the signal (See Column 5 Lines 44-49 of Champaign).

33. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA and Champaign as applied to Claim 3 above, and further in view of Leak.

34. In reference to Claims 5 and 6, AAPA and Champaign teach the limitations as applied to Claim 3 above. AAPA and Champaign do not teach that the delay circuit is an asynchronous delay circuit comprising an even number of inverters connected in series, wherein a first of said even number of inverters receives said first bus access request signal and a last of said even number of inverters generates said time-delayed first bus access request signal. Leak teaches an asynchronous delay chain comprising an even number of inverters wherein the first inverter in the chain receives a signal at its input and the last inverter in the chain generates a time-delayed version of the input signal (See Figure 1 and Column 4 Lines 3-37).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of AAPA and Champaign using the delay chain of Leak, resulting in the inventions of Claims 5 and 6, because a delay chain is simpler to construct than a flip-flop; a delay chain does not require a clock signal; and the switching time of an inverter in a delay chain is faster than the clock signal used by a flip-flop, thus providing a higher resolution when setting the delay time. Further, the delay chain of Leak is used for an equivalent purpose as the delay circuit of Champaign, namely providing a signal to one input of a comparison circuit and providing a delayed version of said signal to the other input of said comparison circuit (See Figure 1 and Column 4 Lines 3-55 of Leak; and Figure 2 and Column 5 Lines 44-48 of Champaign).

35. Claims 1-4, 7-8, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA and US Patent Number 3,886,543 to Marin ("Marin").

36. In reference to Claim 1, AAPA teaches a shared bus system comprising a plurality of bus devices capable of requesting access to a shared bus (See Figure 2), a bus arbitrator (See Figure 2 Number 210) operable to slowly activate and rapidly de-activate tristate line drivers (See Figure 2 Numbers 230A and 230B) coupled to said shared bus (See Figure 2 Number 240), said bus arbitrator comprising: an input circuit (See Figure 2 Numbers 215 and 220) capable of receiving a first bus access request signal (See Figure 2 'REQ1') from a first of said plurality of bus devices and a second bus access request signal (See Figure 2 'REQ2') from a second of said plurality of bus devices, the input circuit also capable of outputting the second bus access request signal when the first bus access request signal is not enabled and blocking the second bus access request signal when the first bus access request signal is enabled (See Figure 2 Numbers 215 and 220). AAPA does not teach a delay circuit capable of receiving a first bus access request signal and generating therefrom a time-delayed first bus access request signal; and a comparator circuit capable of receiving said first bus access request signal and said time-delayed first bus access request signal and generating a line driver enable signal only if both of said first bus access request signal and said time-delayed first bus access request signal are enabled. Marin teaches a delay circuit (See Figure 2 Number 50 and Column 7 Lines 46-52) capable of receiving a signal (See Figure 2 Letter A) and generating therefrom a time-delayed signal (See Figure 2 Letter B); and a comparator circuit capable of receiving said signal and said time-delayed signal and generating a line driver enable signal only if both of said signal

and said time-delayed signal are enabled (See Figure 2 Number 62 and Column 7 Lines 46-52).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of AAPA with the delay system of Marin, resulting in the invention of Claim 1, in order to provide a debounce delay period which ensures that the signal has reached a steady state and thus increases the fault tolerance (See Column 7 Lines 50-52 of Marin).

37. In reference to Claim 2, AAPA and Marin teach the limitations as applied to Claim 1 above. Marin further teaches using an AND gate as the comparator circuit for comparing the signal and the delayed signal, and thus the output of the AND gate will inherently be disabled if either the signal or the delayed signal is disabled, since the output of an AND gate is only enabled when all of its inputs are enabled (See Figure 2 Number 62 and Column 7 Lines 50-59).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of AAPA with the delay system of Marin, resulting in the invention of Claim 2, in order to provide a debounce delay period which ensures that the signal has reached a steady state and thus increases the fault tolerance (See Column 7 Lines 50-52 of Marin).

38. In reference to Claim 3, AAPA and Marin teach the limitations as applied to Claim 2 above. Marin further teaches that the time delay of the delay circuit is equal to the

time for shifting the input through a shift register, which is inherently much greater than the maximum de-activation delay period, which is equivalent to the switching time of the AND gate (See Figure 2 Number 50 and Column 7 Lines 46-50).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of AAPA with the delay system of Marin, resulting in the invention of Claim 3, in order to provide a debounce delay period which ensures that the signal has reached a steady state and thus increases the fault tolerance (See Column 7 Lines 50-52 of Marin).

39. In reference to Claim 4, AAPA and Marin teach the limitations as applied to Claim 3 above. Marin further teaches that said comparator circuit comprises an AND gate having a first input for receiving said signal and a second input for receiving said time-delayed signal (See Figure 2 Number 62 and Column 7 Lines 56-61).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of AAPA with the delay system of Marin, resulting in the invention of Claim 4, in order to provide a debounce delay period which ensures that the signal has reached a steady state and thus increases the fault tolerance (See Column 7 Lines 50-52 of Marin).

40. In reference to Claims 7 and 8, AAPA and Marin teach the limitations as applied to Claim 3 above. Marin further teaches that said delay circuit is a synchronous delay circuit which comprises a flip-flop having an input capable of receiving said first signal

and an output coupled to said comparator circuit that generates said time-delayed first signal (See Figure 2 Number 50 and Column 7 Lines 46-50).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of AAPA with the delay system of Marin, resulting in the inventions of Claims 7 and 8, in order to provide a debounce delay period which ensures that the signal has reached a steady state and thus increases the fault tolerance (See Column 7 Lines 50-52 of Marin).

41. In reference to Claim 21, AAPA and Marin teach the limitations as applied to Claim 1 above. AAPA further teaches that the input circuit comprises an inverter capable of receiving and inverting the first bus access request signal (See Figure 2 Number 215); and an AND gate capable of receiving the inverted first bus access request signal and the second bus access request signal (See Figure 2 Number 220), the AND gate also capable of outputting the second bus access request signal when the first bus access request signal is not enabled and blocking the second bus access request signal when the first bus access request signal is enabled (See Figure 2 Number 210).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of AAPA with the delay system of Marin, resulting in the invention of Claim 21, in order to provide a debounce delay period which ensures that the signal has reached a steady state and thus increases the fault tolerance (See Column 7 Lines 50-52 of Marin).

42. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA and Marin as applied to Claim 3 above, and further in view of Leak.

43. In reference to Claims 5 and 6, AAPA and Marin teach the limitations as applied to Claim 3 above. AAPA and Marin do not teach that the delay circuit is an asynchronous delay circuit comprising an even number of inverters connected in series, wherein a first of said even number of inverters receives said first bus access request signal and a last of said even number of inverters generates said time-delayed first bus access request signal. Leak teaches an asynchronous delay chain comprising an even number of inverters wherein the first inverter in the chain receives a signal at its input and the last inverter in the chain generates a time-delayed version of the input signal (See Figure 1 and Column 4 Lines 3-37).

44. It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of AAPA and Marin using the delay chain of Leak, resulting in the inventions of Claims 5 and 6, because a delay chain is simpler to construct than a flip-flop; a delay chain does not require a clock signal; and the switching time of an inverter in a delay chain is faster than the clock signal used by a flip-flop, thus providing a higher resolution when setting the delay time. Further, the delay chain of Leak is used for an equivalent purpose as the shift register delay circuit of Marin, namely providing a signal to one input of a comparison circuit and providing a

delayed version of said signal to the other input of said comparison circuit (See Figure 1 and Column 4 Lines 3-55 of Leak; and Figure 2 and Column 7 Lines 46-50 of Marin).

45. Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wood as applied to Claim 11 above and further in view of Leak.

46. In reference to Claims 13 and 14, Wood teaches the limitations as applied to Claim 11 above. Wood does not teach that the delay circuit is an asynchronous delay circuit comprising an even number of inverters connected in series, wherein a first of said even number of inverters receives said first bus access request signal and a last of said even number of inverters generates said time-delayed first bus access request signal. Leak teaches an asynchronous delay chain comprising an even number of inverters wherein the first inverter in the chain receives a signal at its input and the last inverter in the chain generates a time-delayed version of the input signal (See Figure 1 and Column 4 Lines 3-37).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Wood using the delay chain of Leak, resulting in the inventions of Claims 13 and 14, because a delay chain is simpler to construct than a flip-flop; a delay chain does not require a clock signal; and the switching time of an inverter in a delay chain is faster than the clock signal used by a flip-flop, thus providing a higher resolution when setting the delay time. Further, the delay chain of Leak is used for an equivalent purpose as the flip-flop delay circuit of

Wood, namely providing a signal to one input of a comparison circuit and providing a delayed version of said signal to the other input of said comparison circuit (See Figure 1 and Column 4 Lines 3-55 of Leak; and Figure 3B and Column 3 Lines 43-52 of Wood).

Drawings

47. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: Figure 4 Number 431 and Figure 6 Number 605. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the Examiner, the Applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Response to Arguments

48. Applicant's arguments filed 1 October 2004 with respect to Claims 1-21 have been fully considered but are moot in view of the new ground(s) of rejection. Applicant has significantly modified the scope of the claims and, as shown above, such changes are not persuasive to overcome a rejection based upon 35 USC §§102 and 103. The new ground(s) of rejection presented in this Office action in reference to the aforementioned claims have been necessitated by the Applicant's amendment.

49. In reference to Applicant's arguments with regard to Claims 9 and 17, the Examiner notes that, as shown in the above rejections, Wood teaches a resistor (See Figure 3B Number 66) that keeps the bus at a high logic level when all of the drivers are in a high-impedance state (See Column 3 Lines 41-42).

Conclusion

50. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Thomas J. Cleary whose telephone number is 571-272-3624. The Examiner can normally be reached on Monday-Thursday (7-3:30), Alt. Fridays (7-2:30).

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Mark H. Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TJC

MARK H. RINEHART
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Thomas J. Cleary
Patent Examiner
Art Unit 2111